

## CLAIMS

What is claimed is:

- 1        1.        An integrated circuit (IC) including at least one combinational logic path, said at  
2        least one combinational logic path comprising a plurality of logic blocks, at least one of  
3        said logic blocks being a first type cell and at least one other of said logic blocks being a  
4        second type cell, a fabrication parameter having a first effect on said first type cell and a  
5        second effect on said second type cell.
- 1        2.        An IC as in claim 1 wherein said second effect is opposite said first effect.
- 1        3.        An IC as in claim 2 wherein said logic blocks are CMOS logic circuits, each  
2        comprising one or more field effect transistors (FETs).
- 1        4.        An IC as in claim 3 wherein at least one said first type cell includes at least one  
2        FET tied off.
- 1        5.        An IC as in claim 3 wherein said first cell type is a dense cell type, FET gates  
2        being on contact pitch within each said dense cell.
- 1        6.        An IC as in claim 5 wherein said second cell type is an isolated cell type, FET  
2        gates being on a pitch greater than said contact pitch within each said isolated cell.
- 1        7.        An IC as in claim 4 wherein said fabrication parameter is focus variation for an  
2        FET gate layer.
- 1        8.        An IC as in claim 7 wherein said first effect is an increase in block delay from  
2        said FET gate layer being printed out of focus.

1        9.        An IC as in claim 8 wherein said first cell type is a dense cell type, FET gates  
2        being on contact pitch within each said dense cell and said second cell type is an isolated  
3        cell type, FET gates being on a pitch greater than said contact pitch within each said  
4        isolated cell, whereby cumulative increase in block delay for each said dense cell in said  
5        at least one combinational logic path is offset by cumulative decrease in block delay for  
6        each said isolated cell in said at least one combinational logic path.

1        10.        An IC as in claim 8 further comprising at least one second combinational logic  
2        path, said at least one second combinational logic path consisting of a plurality dense  
3        logic cells, power in said at least one second logic path being reduced from said FET gate  
4        layer being printed out of focus.

1        11.        An IC as in claim 1 wherein IC is a standard cell IC.

1        12.        An integrated circuit (IC) including at least one combinational logic path, said at  
2        least one combinational logic path comprising a plurality of logic blocks, at least one  
3        layer in said at least one logic path having areas of contacted pitch shapes and areas of  
4        shapes spaced wider than said contacted pitch.

1        13.        An IC as in claim 12 wherein said logic blocks are CMOS logic circuits, each  
2        comprising one or more field effect transistors (FETs).

1        14.        An IC as in claim 13 wherein logic blocks include at least one dense cell and at  
2        least one isolated cell, said contacted pitch shapes being in dense cells, delay changes in  
3        said dense cells from said at least one layer printing out-of-focus being offset by delay  
4        changes in isolated cells.

1        15.        An IC as in claim 14 wherein said delay changes in said dense cells are increases  
2        in dense cell delays.

1        16.     An IC as in claim 14 wherein at least one said dense cell is the same logic circuit  
2        as at least one said isolated cell.

1        17.     An IC as in claim 14 wherein said at least one layer is a FET gate layer.

1        18.     An IC as in claim 17 wherein at least one said dense cell includes at least one  
2        shape not included in a logic circuit, FET gates in said dense cell being on said contacted  
3        pitch with said at least one shape and, being on a pitch wider than said contacted pitch  
4        without said at least one shape.

1        19.     An IC as in claim 18 wherein said at least one shape in at least one said dense cell  
2        is the gate of an FET tied off.

1        20.     An IC as in claim 14 further comprising at least one second combinational logic  
2        path, said at least one second combinational logic path consisting of a plurality dense  
3        logic cells, power in said at least one second logic path being reduced from said FET gate  
4        layer being printed out of focus.

1        21.     An IC as in claim 12 wherein IC is a standard cell IC.

1        22.     A standard cell CMOS integrated circuit (IC) chip, at least one combinational  
2        logic path comprising a plurality of standard cell logic blocks, said plurality of logic  
3        blocks including at least one dense cell and at least one isolated cell, gate layer shapes in  
4        said dense cell being on a contacted pitch and gate layer shapes in said isolated cell being  
5        on a pitch wider than said contacted pitch, whereby delay changes in said dense cells  
6        from said gate layer shapes being printed out-of-focus being offset by delay changes in  
7        isolated cells.

- 1 23. A standard cell CMOS IC chip as in claim 22 wherein said logic blocks are logic  
2 circuits, each comprising one or more field effect transistors (FETs).
- 1 24. An standard cell CMOS IC chip as in claim 23 wherein said delay changes in said  
2 dense cells are increases in dense cell delays.
- 1 25. An standard cell CMOS IC chip as in claim 24 wherein at least one said dense cell  
2 is the same logic circuit as at least one said isolated cell.
- 1 26. An standard cell CMOS IC chip as in claim 24 wherein at least one said dense cell  
2 includes at least one shape not included in a logic circuit, FET gates in said dense cell  
3 being on said contacted pitch with said at least one shape and, being on a pitch wider than  
4 said contacted pitch without said at least one shape.
- 1 27. An standard cell CMOS IC chip as in claim 26 wherein said at least one shape in  
2 at least one said dense cell is the gate of an FET tied gate to source.
- 1 28. An standard cell CMOS IC chip as in claim 23 further comprising at least one  
2 second combinational logic path, said at least one second combinational logic path  
3 consisting of a plurality dense logic cells, power in said at least one second logic path  
4 being reduced from said FET gate layer being printed out of focus.